Design of Power Efficient 4:2 Compressors Using PFAL and Modified PFAL Adiabatic Logic Families

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***Abstract*- Compressor is a crucial entity for all multiplier circuits, which influence the speed of operation of the circuit. This paper presents the low power design of a 4:2 compressor in adiabatic *logic* style. Two adiabatic logic families namely, positive feedback adiabatic logic (PFAL) and modified PFAL are chosen over the other adiabatic families due to their ease in CMOS integration in deep sub-micron technologies. The proposed compressor designs are implemented and their functionality is verified through simulations in Tanner EDA simulator using 180nm CMOS parameters. An investigation on the power consumption of the proposed compressor by varying the power supply, load capacitance and frequency of the signal is done. It is found that the modified PFAL based 4:2 compressor shows the best performance.**

***Keywords*- Adiabatic logic, PFAL, Modified PFAL, VLSI, Compressor, Power Efficient Circuits**

1. INTRODUCTION

In today's world, while moving towards digitalization of data and circuits, power consumption has become major concern in design of portable devices [1]. The digitization of data involves extensive processing resulting in power hungry devices. Portable devices like laptops, cell phones, therefore require the circuitries that consume low power. CMOS logic is generally employed in designing digital circuits due to design ease, high speed. But in relation to battery operated devices, there is a need to lower power consumption of devices. New methodologies have been developed in the past to reduce the losses in the CMOS circuits at various levels of abstraction such as voltage scaling, compact layout, clock gating etc. [2]. However, it has been proven that the circuit design using adiabatic logic has the potential to reduce power consumed per operation significantly [1].

Along with the low power requirement, now-a-days a majority of applications require high speed data computation units. High speed multipliers play a potent role in designing such digital circuits [3]. They are used in real time image and speech processing, mainly the fields where high speed and accuracy is required [4]. Consequently, many methods have been suggested to make multiplication fast and accurate [5]. It is noted that the partial product reduction stage is responsible for a significant portion of the total multiplication delay, power and area. To address this issue, compressors are usually employed since they reduce partial products thereby reducing the critical path to maintain the circuit's performance [6]. Today, majority of the multiplier designs use 4:2 compressors to speed up the partial product summation

tree [7]. In this paper, we propose compressor design in adiabatic logic style. As there are varieties of adiabatic logic families [8], the compressor design in positive feedback adiabatic logic (PFAL) is adopted due to its suitability to CMOS integration in deep sub-micron technologies. The power consumption is further lowered by designing the compressor using modified PFAL (MPFAL) style.

This paper is organized in five section including the introductory one. Section II briefly describes the adiabatic logic style and the two families. The compressor design is proposed in section III. The functional verification of the design and the performance comparison is presented section IV. The conclusions are drawn in the last section.

2.ADIABATIC LOGIC CIRCUITS

The schematic of a CMOS inverter consisting of NMOS (M1) and PMOS (M2) representing the pull-down and pull-up networks are shown in Fig. 1. Depending on the input either M1 or M2 is ON while the other remains OFF [9]. The inverter consumes power when the input switches from V_{DD} to 0 and charges the output capacitor C_1 whereas it dissipates the power via M1 in a discharging event initiated by the switching of the input from 0 to V_{DD}. The dynamic power consumption of the CMOS inverter is expressed as:

$$P_{dyn} = \alpha . C_1 . V_{DD}^2 . f \quad (1)$$

where, α, C_1, V_{DD} and f represents the switching activity, load capacitance, power supply and frequency of the input. Various methodologies to reduce the values of the factors are suggested as low power solutions for CMOS circuits. But adiabatic logic has been proven to be a potential solution over CMOS logic style when it comes to design of low power circuits [1]. In contrast to CMOS, adiabatic logic does not switch abruptly from 0 to V_{DD} or vice versa but employ a slow changing voltage to charge and recover the energy from the output.

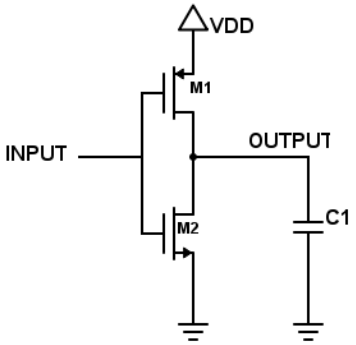

Fig.1: CMOS Inverter

Two adiabatic logic families namely positive feedback adiabatic logic (PFAL) [10,11] and modified positive feedback adiabatic logic (MPFAL) [12] are considered. The basic cell in PFAL is shown in Fig. 2. The logic function F and its complement Fbar are implemented using NMOS networks alongside the two cross coupled inverters as latch which drives the two complementary outputs of the circuit. It requires presence of dual nature of input and creates dual nature as well which increases its compatibility [11].

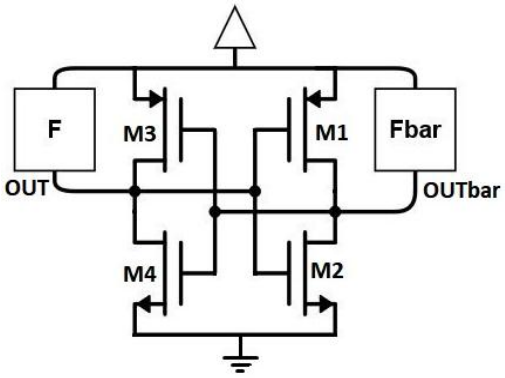

Fig.2: Basic Cell of PFAL [10]

Another enhanced version of the PFAL family is shown in Fig. 3 and is named as modified PFAL (MPFAL) [12]. A basic MPFAL gate has a latch with two cross

coupled inverters (M1-M4) similar to PFAL and an additional diode connected NMOS transistor M5, in between the source of PFAL cross coupled inverters and round terminal that helps in reducing power dissipation [13]. MPFAL is based on level shifting technique which has one power clock supply and a NMOS transistor. The logic function is realized in the similar manner as the PFAL thus the number of transistors remains same as that in PFAL for realizing the logic function.

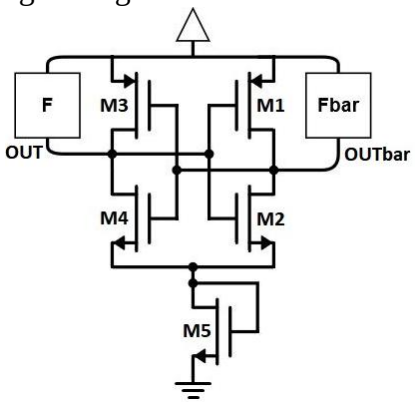

Fig.3: Basic Cell of MPFAL [12]

Both of these logics use four phase power supply (Fig. 4) with the phases as: evaluate, hold, recovery and wait state [1]. In the evaluate phase, the outputs are evaluated from the stable inputs while the outputs are kept stable for the evaluation of the next stage in the hold phase. The energy is recovered in the recovery phase and an extra wait phase has been added to maintain symmetry.

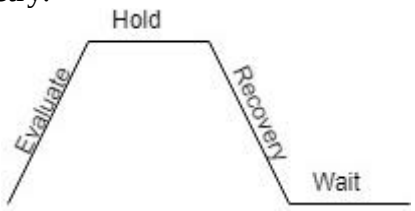

Fig.4: Four Phase Trapezoidal Power Supply [1]

3. PROPOSED COMPRESSOR

Major applications of electronics devices, today, desire high speed computation of data, which includes a multiplication unit [14]. An array multiplier is a fast multiplier architecture. It consists of three parts: a partial product summation tree, booth encoder and a final adder [15]. The partial product summation tree is responsible for total delay in multiplication procedure. Various techniques are available that helps in speeding up the partial product summation tree. One of these is column compressors since they simplify the interconnection circuitry [16]. The realization of a 4:2 compressor with five inputs (X1, X2, X3, X4, Cin) and three outputs (Sum, Carry, cout) is considered. The truth table of the compressor is listed in Table I [19]. The block diagrams of two compressors design (Compressor A [17] and Compressor B [18]) are depicted in Fig. 5 and Fig. 6. The functionality of 4:2 Compressor A can be expressed as:

$$\textbf{\textit{Sum}}=X1 \oplus X2 \oplus X3 \oplus X4 \oplus Cin \quad (2)$$

$$\textbf{\textit{Carry}}=(X1 \oplus X2 \oplus X3 \oplus X4).Cin+\overline{(X1 \oplus X2 \oplus X3 \oplus X4)}.X4 \quad (3)$$

$$\textbf{\textit{Cout}}= (X1 \oplus X2).X3 + \overline{(X1 \oplus X2)}.X1 \quad (4)$$

TABLE I: TRUTH TABLE OF 4:2 COMPRESSOR

C_{in}	X_4	X_3	X_2	X_1	C_{out}	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1

1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

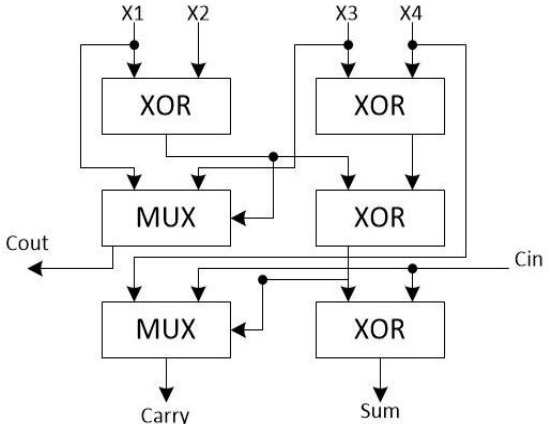

Fig. 5. Block Diagram of 4:2 Compressor A [17]

Similarly, the Boolean expression of the 4:2 Compressor B can be written as follows:

Sum=$(X1 \oplus X2).\overline{(X3 \oplus X4)} + \overline{(X1 \oplus X2)}.(X3 \oplus X4.Cin + (X1 \oplus X2).(X3 \oplus X4) + X1 \oplus X2.X3 \oplus X4.Cin$ (5)

Carry=$(X1 \oplus X2 \oplus X3 \oplus X4).Cin + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)}.X4$ (6)

Cout=$(X1 \oplus X2).X3 + \overline{(X1 \oplus X2)}.X1$ (7)

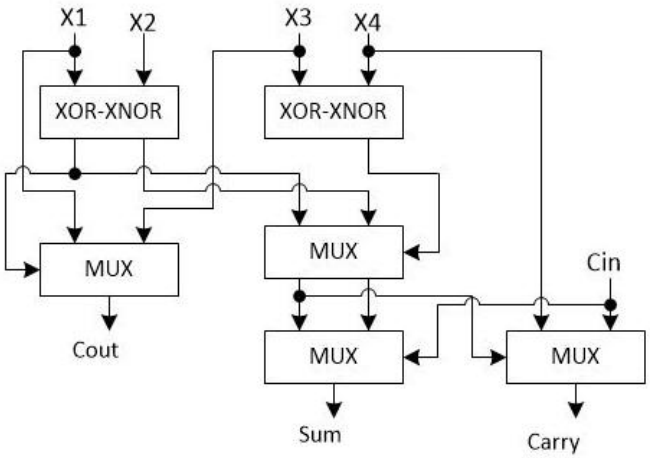

Fig.6: Block Diagram of 4:2 Compressor B [18]

It is clear from Figs. 5 and 6 that both the compressors use 2:1 multiplexer (MUX) [20] and exclusive-OR (XOR) gates as building blocks. The functionality of 2:1 MUX is expressed as:

$$OUT = A.Sbar + B.S \quad (9)$$

The functionality of XOR gate is expressed as:

$$XOR = A \oplus B = A.Bbar + Abar.B \quad (10)$$

The functionality of XOR gate is expressed as:

$$XNOR = A \odot B = A.B + Abar.Bbar \quad (11)$$

The Compressor A design consists of 2 MUX and 4 XOR blocks whereas the Compressor B design consists of 4 MUX and 2 XOR blocks. The PFAL based 2:1 MUX and XOR gate are shown in Figs. 7 and Fig. 8 respectively. A 2:1 multiplexer [21] contains two inputs A, B and one select line S and outputs OUT and OUTbar as shown in Fig. 7. The logic function has been realized using NMOS transistors only and both inputs and complemented inputs are applied. Similarly, XOR gate uses two inputs A and B supplied in true and complementary form to the NMOS network. The MPFAL based implementations of 2:1 MUX and XOR gate are shown in Fig. 9 and Fig. 10 respectively.

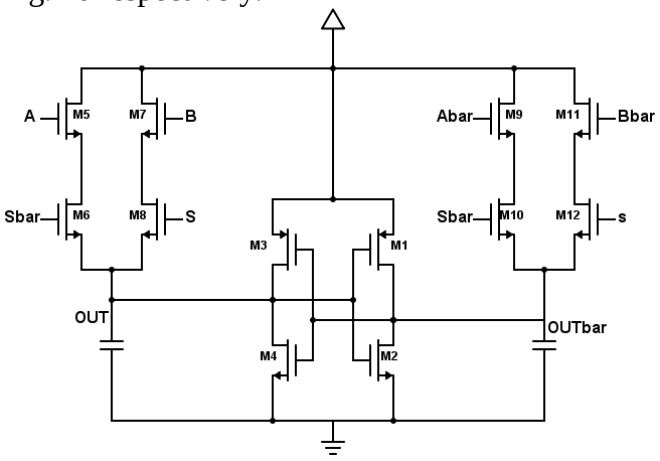

Fig.7: Proposed PFAL 2:1 MUX

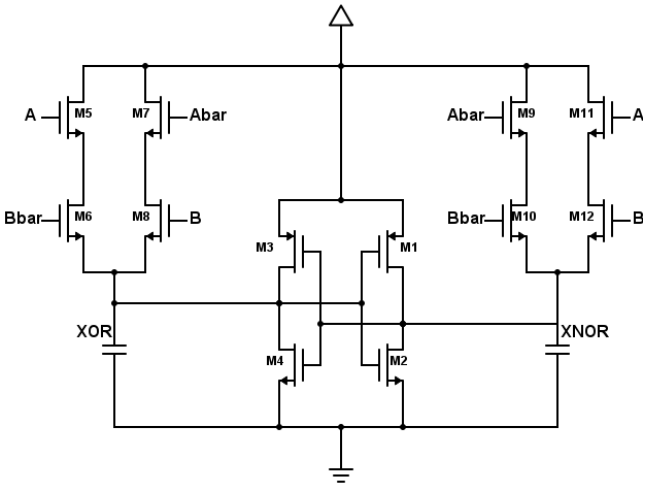

Fig.8: Proposed PFAL XOR gate

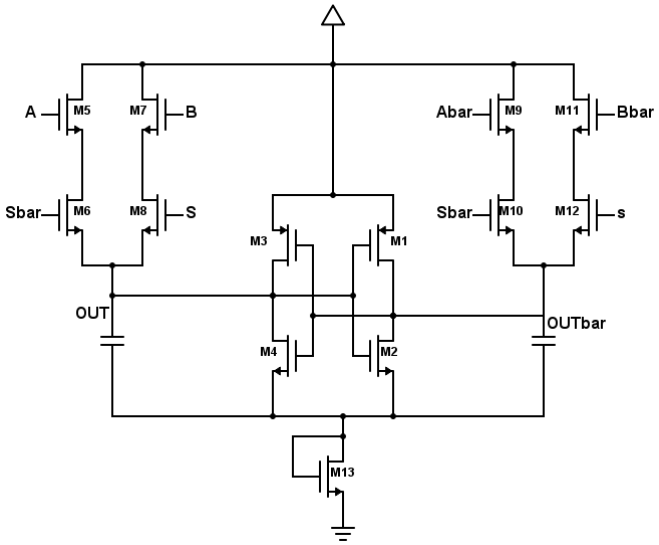

Fig.9: Proposed MPFAL 2:1 MUX

4. Simulation Results

The circuits for the 4:2 Compressor based on two designs Compressor A (Fig. 5) and Compressor B (Fig. 6) are designed in PFAL and MPFAL styles. Both the compressor designs are implemented and simulated in Tanner EDA using 180 nm CMOS technology parameters. For PFAL based design, the MUX and XOR gate circuits shown in Fig. 7 and Fig. 8 are used while for MPFAL, the circuits of Fig. 9 and Fig. 10 are employed. This section first presents the functional verification of the

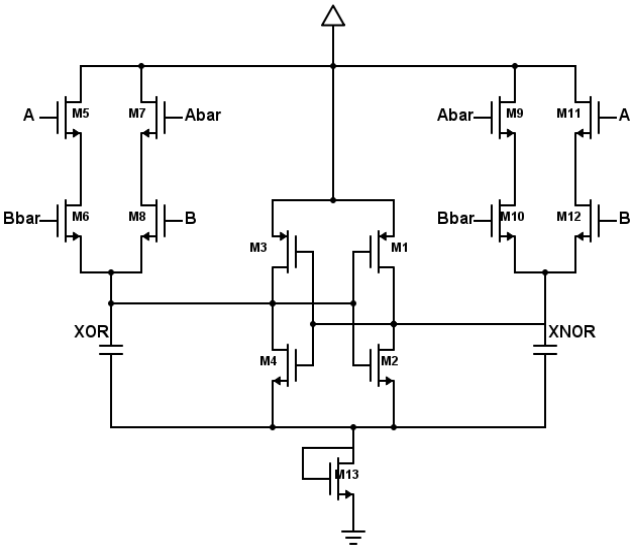

Fig.10: Proposed MPFAL XOR gate

compressors, thereafter their performance is compared with their CMOS counterparts, in terms of power for wide range of power supply, capacitance and input frequency value.

A. Verification of Compressor Functionality

The two compressors are implemented and simulated with a power supply, load capacitance, input frequency of 1.8 V, 10 fF and 25MHz respectively. The simulation waveforms for compressor A implemented in PFAL and MPFAL are plotted in Fig. 11 and Fig.12 respectively. Similar waveforms were obtained for compressor B and are not shown for the sake of brevity. It can be observed that the compressors exhibit the same functionality as predicted in Table I.

B. Power Dissipation Analysis With Power Supply

The power dissipation of the two proposed compressors A and B are measured by varying the supply voltages from 1V to 2V. The load capacitance and input frequency are maintained constant at 10fF and 25MHz respectively. The simulation results are plotted in Fig. 13 and

Fig. 14 for Compressor A and Compressor B respectively. The values of power consumption are listed in Table III. It can be observed that both the adiabatic implementation of the compressors consumes lesser power than the CMOS counterparts. Thus, identifying adiabatic logic as a low power style. Also, the power consumption in both the logic style increases with the increment in power supply. However, the increase in adiabatic family is not that sharp as observed in CMOS logic. Also, it may be observed that proposed Compressor B has a lower power dissipation compared to Compressor A. With respect to the logic family, MPFAL based compressor design show low power dissipation values than their PFAL implementations. Overall, Compressor B implemented using MPFAL had lowest power dissipation. CMOS circuits show the highest power consumption amongst the three logic families.

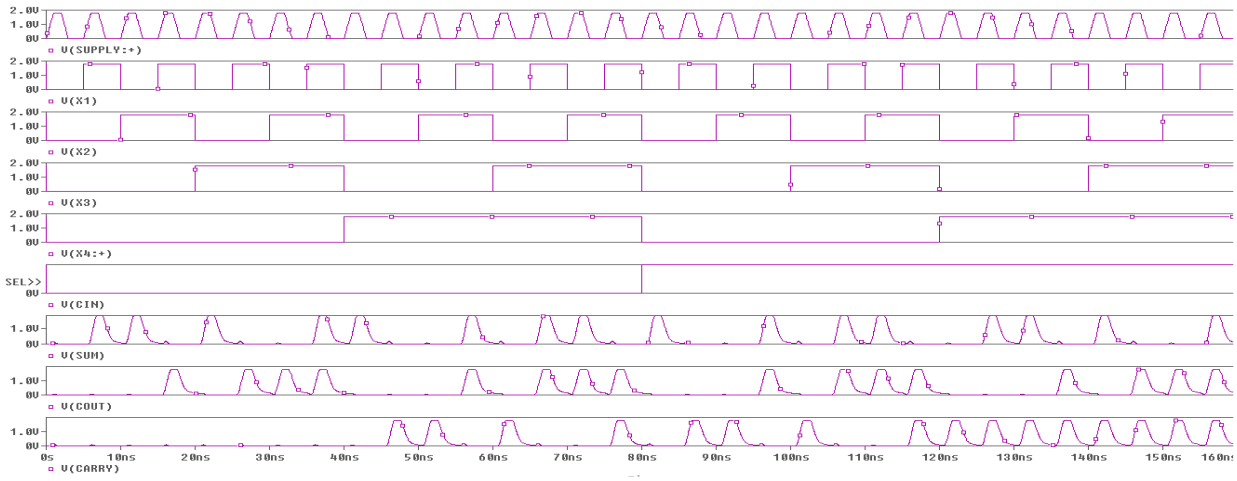

Fig.11: Simulation Waveform of PFAL Compressor A

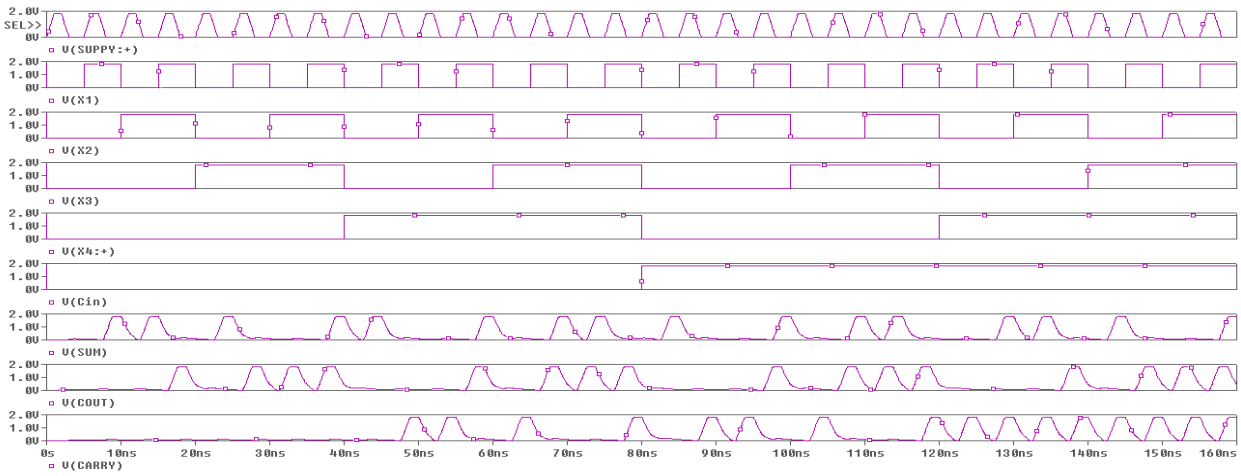

Fig.12: Simulation waveform of MPFAL Compressor A

TABLE III: POWER VS. POWER SUPPLY FOR PROPOSED COMPRESSORS A AND B

Supply Voltage (V)	COMPRESSOR A (µW)			COMPRESSOR B (µW)		
	PFAL	MPFAL	CMOS	PFAL	MPFAL	CMOS
1	0.61	0.51	0.98	0.58	0.52	0.93
1.1	0.64	0.57	1.61	0.61	0.54	1.13
1.2	0.68	0.61	2.25	0.69	0.61	1.35
1.3	0.78	0.64	2.23	0.72	0.62	2.08
1.4	0.83	0.70	3.62	0.83	0.76	2.65
1.5	0.93	0.76	3.83	0.94	0.82	3.62
1.6	1.09	0.92	4.46	1.05	0.94	4.13
1.7	1.28	1.06	5.23	1.17	1.02	4.57
1.8	1.58	1.22	5.86	1.43	1.18	4.91
1.9	1.83	1.36	6.53	1.59	1.33	5.48
2	1.02	1.52	7.54	1.91	1.58	5.89

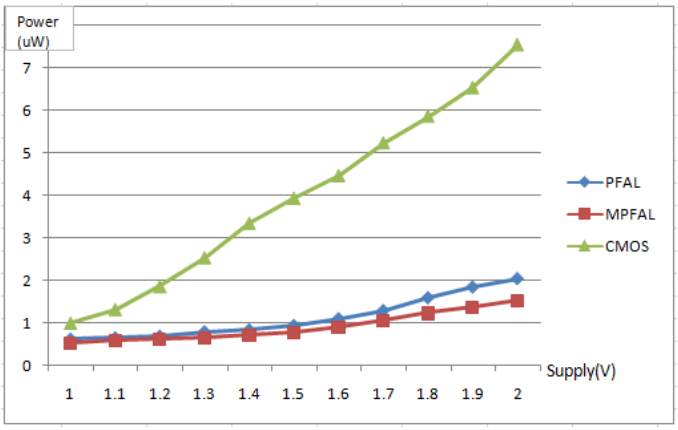

Fig.13: Power Dissipation vs. Power Supply for Proposed Compressor A

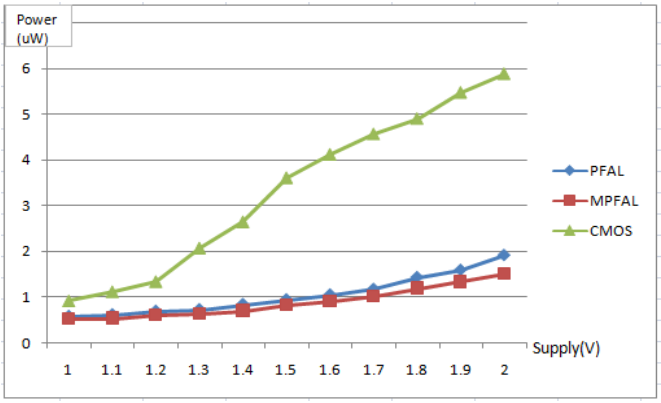

Fig.14: Power Dissipation vs. Power Supply for Proposed Compressor B

C. Power Dissipation Analysis With Varying Load Capacitances

The power dissipation of the proposed compressors A and B are measured for various load capacitances ranging from 1fF to 200fF while keeping the power supply voltage constant at 1.8 V. The simulation results are plotted for the compressors implemented in CMOS, PFAL and MPFAL are plotted in Fig. 15 and Fig. 16. It may be observed that compressor B consumes less power than the rest of the two circuits. The exact values are listed in Table IV. Initially, for capacitance values from 1fF to 40fF, all the four adiabatic compressors have almost same power dissipation but as the load capacitance increases, the proposed compressor B design using MPFAL shows the best performance amongst all the compressors. CMOS based compressors show highest power values at all values of load capacitance.

TABLE IV: POWER VS. LOAD CAPACITANCES FOR PROPOSED COMPRESSORS A AND B

Load Capacitance (fF)	COMPRESSOR A (µW)			COMPRESSOR B (µW)		
	PFAL	MPFAL	CMOS	PFAL	MPFAL	CMOS
1	1.23	1.35	3.49	1.19	1.36	2.56
2	1.22	1.21	3.74	1.98	1.32	2.80
5	1.27	1.12	4.46	1.49	1.21	4.01
10	1.38	1.02	5.66	1.93	1.23	4.11
20	2.07	1.87	8.03	2.26	1.62	7.02
30	3.25	2.81	10.44	3.29	2.68	8.91
40	4.64	3.85	12.83	4.46	3.83	11.31
50	6.19	4.89	15.26	6.47	4.86	13.73
60	7.86	6.06	17.71	7.99	6.23	16.14
80	10.85	8.59	22.56	11.41	8.57	20.93
100	16.32	11.39	27.42	14.91	11.81	31.73
150	24.67	19.62	39.53	24.72	19.54	40.78
200	36.01	29.21	51.66	36.34	28.83	49.69

D. Power Dissipation Analysis With Varying Frequency

The dependence of power dissipation on frequency is examined by simulating the compressor designs at supply voltage of 1.8

V and keeping load capacitance at 10 fF. The input frequency is varied from 12.5 MHz to 250 MHz. The simulation results are plotted in Fig. 17 and Fig. 18 for proposed Compressor A and B. It is observed from the graph that power dissipation is lower in Compressor B than Compressor A. At the beginning, at around 12.5MHz to 40MHZ, all the four adiabatic compressors have almost the same power dissipation. The exact values are listed in Table V. Here also, CMOS compressors show large power dissipation and it increases as the frequency value is increased. The adiabatic compressors show low power consumption than CMOS till 200MHZ after that gap between their power consumptions starts to decrease. Compressor B, designed using Modified PFAL shows the best performance amongst all the designed compressors.

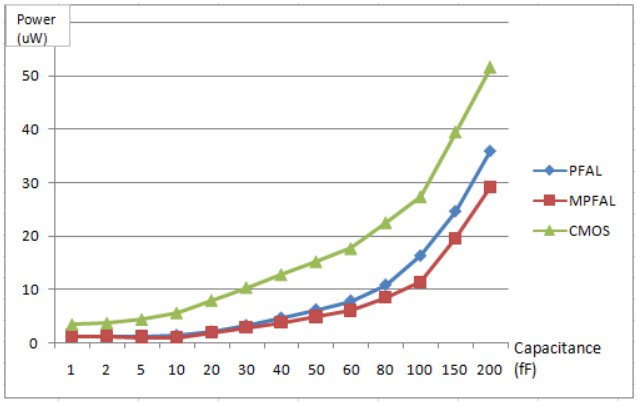

Fig.15: Power Dissipation vs. Load Capacitance for Proposed Compressor A

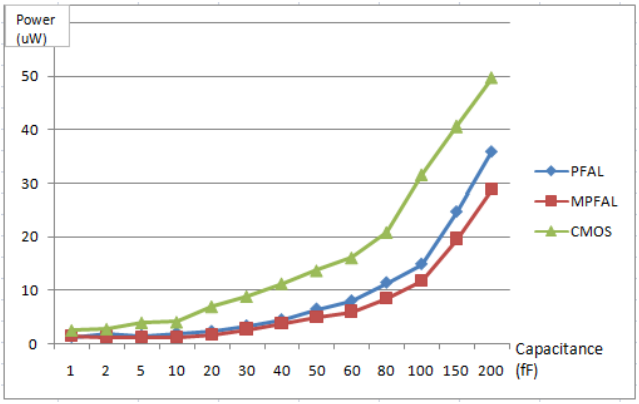

Fig.16: Power Dissipation vs. Load Capacitance for Proposed Compressor B

TABLE V: POWER VS. FREQUENCY FOR PROPOSED COMPRESSORS A AND B

Frequency (MHz)	COMPRESSOR A (µW)			COMPRESSOR B (µW)		
	PFAL	MPFAL	CMOS	PFAL	MPFAL	CMOS
12.5	0.99	0.38	3.97	0.84	0.59	1.59
25	2.38	0.72	5.66	1.66	1.26	3.91
50	6.25	2.76	9.05	5.42	2.91	9.04
100	9.53	5.12	15.83	10.99	6.86	15.62
125	13.34	8.22	20.48	12.71	8.74	23.48
200	23.61	17.87	29.27	21.98	16.43	28.48
250	34.44	27.13	38.06	31.94	23.50	37.72

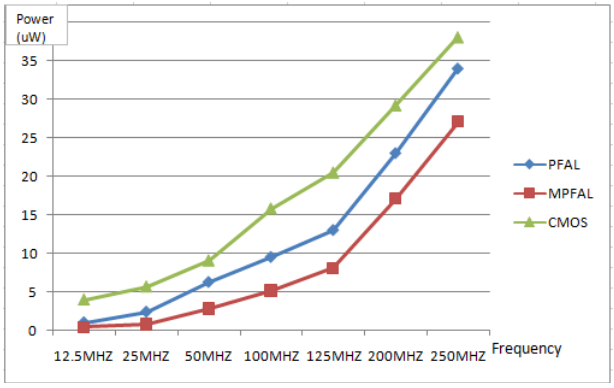

Fig.17: Power Dissipation vs. Input Frequency for Compressor A

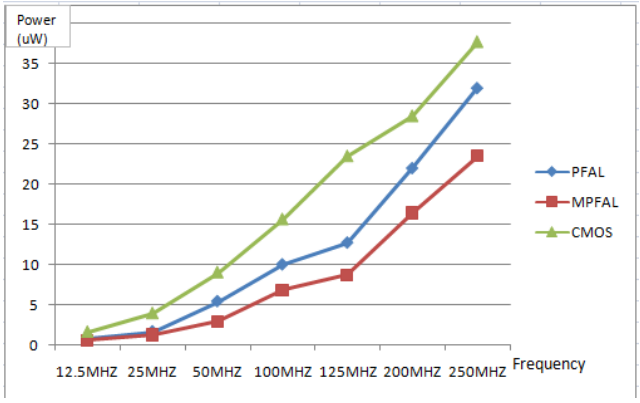

Fig.18: Power Dissipation vs. Input Frequency for proposed compressor B

5. Conclusion

In this paper, compressor designs in adiabatic logic style are proposed. The two adiabatic logic families, positive feedback adiabatic logic (PFAL) and it modified version (MPFAL) are adopted for their

realization. Two realization of 4:2 compressor for each logic family is proposed. The proposed compressor designs are simulated in Tanner EDA simulator using 180nm CMOS parameters. The performance between the circuits is made by varying the power supply, load capacitance and frequency of the signal. It is found that the adiabatic compressor consumes less power than the CMOS counterparts. Also, the modified PFAL based compressor design consumes the lowest power at all conditions.

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